

WHAT IS CLAIMED IS:

1 1. An integrated circuit, comprising:
2 a transistor level comprising one or more semiconductor devices disposed over a
3 substrate and an overlying transistor isolation layer having one or more contact vias
4 extending therethrough;
5 a ferroelectric device level comprising one or more ferroelectric capacitors
6 disposed over the transistor isolation layer and an overlying ferroelectric isolation layer
7 having one or more vias extending therethrough and laterally sized larger than
8 corresponding contact vias aligned therewith;
9 a first metal level disposed over the ferroelectric device level;
10 an inter-level dielectric level disposed over the first metal level; and
11 a second metal level disposed over the inter-level dielectric level.

1 2. The subject matter of claim 1, wherein the contact vias are filled with
2 tungsten contact plugs.

1 3. The subject matter of claim 2, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 4. An integrated circuit, comprising:
2 a transistor level comprising one or more semiconductor devices disposed over a
3 substrate and an overlying transistor isolation layer having one or more contact vias
4 extending therethrough;
5 an integrated first metal and ferroelectric device level comprising one or more
6 first metal contacts and one or more ferroelectric capacitors disposed over the transistor
7 isolation layer and a ferroelectric isolation layer having one or more vias extending
8 therethrough;
9 an inter-level dielectric level disposed over the integrated first metal and
10 ferroelectric device level; and
11 a second metal level disposed over the inter-level dielectric level.

1 5. The subject matter of claim 4, wherein the contact vias are filled with
2 tungsten contact plugs.

1 6. The subject matter of claim 5, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 7. The subject matter of claim 4, wherein the integrated first metal and
2 ferroelectric device level has a thickness corresponding substantially to the ferroelectric
3 capacitor heights.

1 8. The subject matter of claim 4, wherein the integrated first metal and
2 ferroelectric device level is substantially non-planar with a reduced thickness in non-
3 capacitor regions.

1 9. An integrated circuit, comprising:
2 a transistor level comprising one or more semiconductor devices disposed over a
3 substrate and an overlying transistor isolation layer having one or more contact vias
4 extending therethrough;
5 a first metal level disposed over the transistor isolation layer;
6 a ferroelectric device level comprising one or more ferroelectric capacitors
7 disposed over the first metal level and an overlying ferroelectric isolation layer having
8 one or more vias extending therethrough;
9 an inter-level dielectric level disposed over the ferroelectric device level; and
10 a second metal level disposed over the inter-level dielectric level.

1 10. The subject matter of claim 9, wherein the contact vias are filled with
2 tungsten contact plugs.

1 11. The subject matter of claim 10, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 12. An integrated circuit, comprising:
2 a transistor level comprising one or more semiconductor devices disposed over a
3 substrate and an overlying transistor isolation layer having one or more contact vias
4 extending therethrough;
5 a first metal level disposed over the transistor isolation layer;
6 an inter-level dielectric level disposed over the first metal level;

7 a ferroelectric device level comprising one or more ferroelectric capacitors
8 disposed over the inter-level dielectric level and an overlying ferroelectric isolation
9 layer having one or more vias extending therethrough; and
10 a second metal level disposed over the ferroelectric isolation layer.

1 13. The subject matter of claim 12, wherein the contact vias are filled with
2 tungsten contact plugs.

1 14. The subject matter of claim 13, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 15. An integrated circuit, comprising:
2 a transistor level comprising one or more semiconductor devices disposed over a
3 substrate and an overlying transistor isolation layer;
4 a ferroelectric device level comprising one or more ferroelectric capacitors
5 disposed over the transistor isolation layer and an overlying ferroelectric isolation layer
6 having one or more vias extending through the ferroelectric isolation layer and the
7 transistor isolation layer;
8 a first metal level disposed over the ferroelectric device level;
9 an inter-level dielectric level disposed over the first metal level; and
10 a second metal level disposed over the inter-level dielectric level.

1 16. The subject matter of claim 15, wherein the contact vias are filled with
2 tungsten contact plugs.

1 17. The subject matter of claim 16, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 18. A method of forming an integrated circuit, comprising:
2 forming a transistor level comprising one or more semiconductor devices
3 disposed over a substrate and an overlying transistor isolation layer having one or more
4 contact vias extending therethrough;
5 forming a ferroelectric device level comprising one or more ferroelectric
6 capacitors disposed over the transistor isolation layer and an overlying ferroelectric

7 isolation layer having one or more vias extending therethrough and laterally sized larger
8 than corresponding contact vias aligned therewith;

9 forming a first metal level over the ferroelectric device level;

10 forming an inter-level dielectric level over the first metal level; and

11 forming a second metal level over the inter-level dielectric level.

1 19. The subject matter of claim 18, wherein the contact vias are filled with
2 tungsten contact plugs.

1 20. The subject matter of claim 19, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 21. A method of forming an integrated circuit, comprising:

2 forming a transistor level comprising one or more semiconductor devices
3 disposed over a substrate and an overlying transistor isolation layer having one or more
4 contact vias extending therethrough;

5 forming an integrated first metal and ferroelectric device level comprising one or
6 more first metal contacts and one or more ferroelectric capacitors disposed over the
7 transistor isolation layer and a ferroelectric isolation layer having one or more vias
8 extending therethrough;

9 forming an inter-level dielectric level over the integrated first metal and
10 ferroelectric device level; and

11 forming a second metal level over the inter-level dielectric level.

1 22. The subject matter of claim 21, wherein the contact vias are filled with
2 tungsten contact plugs.

1 23. The subject matter of claim 22, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 24. The subject matter of claim 21, wherein the integrated first metal and
2 ferroelectric device level has a thickness corresponding substantially to the ferroelectric
3 capacitor heights.

1 25. The subject matter of claim 21, wherein the integrated first metal and
2 ferroelectric device level is substantially non-planar with a reduced thickness in non-
3 capacitor regions.

1 26. A method of forming an integrated circuit, comprising:
2 forming a transistor level comprising one or more semiconductor devices
3 disposed over a substrate and an overlying transistor isolation layer having one or more
4 contact vias extending therethrough;
5 forming a first metal level over the transistor isolation layer;
6 forming a ferroelectric device level comprising one or more ferroelectric
7 capacitors disposed over the first metal level and an overlying ferroelectric isolation
8 layer having one or more vias extending therethrough;
9 forming an inter-level dielectric level over the ferroelectric device level; and
10 forming a second metal level over the inter-level dielectric level.

1 27. The subject matter of claim 26, wherein the contact vias are filled with
2 tungsten contact plugs.

1 28. The subject matter of claim 27, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 29. A method of forming an integrated circuit, comprising:
2 forming a transistor level comprising one or more semiconductor devices
3 disposed over a substrate and an overlying transistor isolation layer having one or more
4 contact vias extending therethrough;
5 forming a first metal level over the transistor isolation layer;
6 forming an inter-level dielectric level over the first metal level;
7 forming a ferroelectric device level comprising one or more ferroelectric
8 capacitors disposed over the inter-level dielectric level and an overlying ferroelectric
9 isolation layer having one or more vias extending therethrough; and
10 forming a second metal level over the ferroelectric isolation layer.

1 30. The subject matter of claim 29, wherein the contact vias are filled with
2 tungsten contact plugs.

1 31. The subject matter of claim 30, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

1 32. A method of forming an integrated circuit, comprising:
2 forming a transistor level comprising one or more semiconductor devices
3 disposed over a substrate and an overlying transistor isolation layer having one or more
4 contact vias extending therethrough;
5 forming a ferroelectric device level comprising one or more ferroelectric
6 capacitors disposed over the transistor isolation layer and an overlying ferroelectric
7 isolation layer having one or more vias extending through the ferroelectric isolation
8 layer and the transistor isolation layer;
9 forming a first metal level over the ferroelectric device level;
10 forming an inter-level dielectric level over the first metal level; and
11 forming a second metal level over the inter-level dielectric level.

1 33. The subject matter of claim 32, wherein the contact vias are filled with
2 tungsten contact plugs.

1 34. The subject matter of claim 33, wherein the ferroelectric capacitors are
2 formed over respective tungsten contact plugs.

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